REMARKS

Reconsideration and allowance of the subject application are respectfully requested. Claims 1-11 remain pending, claims 1, 4, 8, and 10 being independent. In this Reply, Applicant has made minor amendments to independent claims 1, 4, and 8.

Prior Art Rejection

Claims 1-11 stand rejected under 35 U.S.C. § 103 as allegedly being unpatentable over *Itoh et al.* (U.S. Patent 5,585,817) in view of *Ichikawa et al.* (U.S. Patent 6,127,998). This rejection is respectfully traversed.

The Claimed Invention of Independent Claims 1, 4, 8, and 10

Independent claim 1 is directed to an image display apparatus generally comprising an imaging section and a display section. The imaging section recited in claim 1 includes: photoelectronic conversion devices arranged in the form of a matrix, vertical transfer paths arranged adjacent to the respective columns of the photoelectronic conversion devices, each of the vertical transfer paths transferring signal charges toward a lower end in accordance with vertical driving pulses supplied from the outside, transfer gates for transferring signal charges generated by the photoelectronic conversion devices to the respective vertical transfer paths in accordance with field shift pulses supplied from the outside respectively, and output circuits for converting signal charges arrived at the lower ends of the vertical transfer paths to signals and outputting the signals in parallel column by column of the matrix. The display section recited in independent claim 1 includes: display devices arranged in the form of a matrix, input circuits, and a vertical driving circuit.

Each of the display devices has a signal input terminal and a control signal input terminal, and displays an image represented by signals applied to the signal input terminal thereto at the time of application of driving pulses to the control signal input terminal. The input circuits receive signals output from the imaging section in parallel column by column and output signals corresponding the received signals to the signal input terminals of the display devices via signal buses in parallel column by column of the matrix. The vertical driving circuit outputs the driving pulses to the control signal input terminals of the display devices via control buses line by line of the matrix in a predetermined order.

Independent claim 4 is directed to an image display apparatus comprising an imaging section (as substantially described above with regard to claim 1) and a display section, and further comprising a signal conversion section for processing signals output from the imaging section in parallel column by column and outputting the processed signals in parallel. The input circuits for the display section recited in claim 4 receive signals output from the signal conversion section in parallel and output signals corresponding to the received signals to signal input terminals of the display devices via signal buses in parallel column by column.

Independent claim 8 is directed to an image display apparatus generally comprising an imaging section; a signal conversion section; and a parallel-to-serial conversion section. The imaging section of claim 8 includes: photoelectronic conversion devices arranged in the form of a matrix; vertical transfer paths arranged adjacent to the respective columns of the photoelectronic conversion devices, each of the vertical transfer paths transferring signal charges toward a lower end in accordance with vertical driving pulses supplied from

the outside; transfer gates for transferring signal charges generated by the photoelectronic conversion devices to the respective vertical transfer paths in accordance with field shift pulses supplied from the outside respectively; and output circuits for converting signal charges arrived at the lower ends of the vertical transfer paths to signals and outputting the signals in parallel column by column of the matrix. The signal conversion section processes the signals output in parallel from the imaging section column by column and outputs the processed signals in parallel, and the parallel-to-serial conversion section converts the signals output in parallel from the signal conversion section to serial signals.

Independent claim 10 is directed to a display apparatus comprising: a serial-to-parallel conversion section; a signal conversion section; and a display section. The serial-to-parallel conversion section converts signals serially input thereto to parallel signals for output. The signal conversion section processes the signals output in parallel from the serial-to-parallel conversion section column by column and outputs the processed signals in parallel. The display section includes: display devices arranged in the form of a matrix, each of the display devices having a signal input terminal and a control signal input terminal, and displaying an image represented by signals applied to the signal input terminal thereto at the time of application of driving pulses to the control signal input terminal; input circuits for receiving signals output from the signal conversion section in parallel and outputting signals corresponding the received signals to the signal input terminals of the display devices via signal buses in parallel column by column of the matrix; and a vertical driving circuit for outputting the driving pulses to the control signal input

terminals of the display devices via control buses line by line of the matrix in a predetermined order.

Deficiencies in the Asserted Prior Art Rejection

For at least the following reasoning, Applicant respectfully submits that the asserted grounds of rejection set forth on pages 2-3 of the Office Action fails to establish *prima facie* obviousness of any independent claim, or claim depending therefrom.

In rejecting the independent claims, the Examiner initially alleges on page 2 of the Office Action that "Itoh teaches an image input/output apparatus including an image input section (20) and an image display section (10) arranged in a matrix form." The image input section 20 and the image display section 10 disclosed in *Itoh* include a data drive circuit 302, which is adapted to sequentially drive the columns of pixels, as seen in Fig. 3. By contrast, the imaging section of the image display apparatus recited in claims 1, 4, and 8 is adapted to transfer signals column by column through the vertical transfer paths, the thus transferred signals being developed column by column in parallel from the output circuits. This claimed arrangement eliminates circuitry such as the data drive circuit 302 disclosed in *Itoh*, thus resulting in reduced electric power consumption in the imaging section. The Examiner's reliance on the secondary reference, *Ichikawa*, fails to make up for this deficiency in *Itoh*. Furthermore, the Office Action fails to identify a reference that would suggest modifying *Itoh* in a manner that would satisfy this claimed feature.

In addition, the display section of the apparatus recited in claims 1, 4, and 10 is adapted to receive signals column by column, thus also eliminating the need for a data drive circuit such as the circuit 302 disclosed in *Itoh*.

The Examiner further alleges on page 2 of the Office Action that *Itoh* discloses the photodetective portion in connection with the parallel blocks 109' and 109" and the output voltages $V_{out}1$ and $V_{out}2$. The imaging section of claims 1, 4, and 8, however, includes vertical transfer paths for transferring signals, which were produced by the photoelectric conversion devices, column by column. As shown in Fig. 5 of *Itoh*, the parallel blocks 109' and 109" do not include any vertical transfer paths as defined in independent claims 1, 4, and 8.

According to the Examiner, "Itoh et al teaches the V(out) as it relates to the display section including a transparent electrode (105), a thin film transistor (101), and gate electrodes." As understood from Fig. 2 of *Itoh*, the voltage V_{out} represents signals to which the image input section 20 converts input light. Col. 5, lines 27-40. Upon carefully reviewing *Itoh*, however, it is seen that the image input section 20 is adapted for sensing reflected light 112 of back light 110, and the image display section 10 is adapted for transmitting or blocking the back light 110 in response to input signals to display the input signals. Col. 4, line 66 - col. 5, line 11. Both the image input section 20 and the image display section 10 are thus adapted to utilize the back light 110, therefore failing to operate simultaneously with each other. This precludes data generated by the image input section 20 from being immediately displayed on the image display section 10. In contrast, the

image display apparatus recited in independent claims 1 and 4 allows an image captured by the imaging section to be immediately displayed on the display apparatus.

The Examiner also states on page 2 of the Office Action that "Itoh teaches the supplying of electric signal to a scanning circuit." According to col. 1, lines 53-56 of *Itoh*, such a scanning circuit included in an image input apparatus is adapted for converting an electric signal to a time-serial signal. In accordance with the invention of claims 1, 4, and 8, however, the imaging section comprises the vertical transfer paths transferring signal charges column by column as well as the output circuits outputting the signals thus transferred on the vertical transfer paths in parallel column by column. These claimed features are not suggested by the scanning circuit disclosed by *Itoh* for converting an electric signal to a time-serial signal.

Regarding the secondary reference, the Examiner asserts on pages 2-3 of the Office Action that *Ichikawa* teaches a light receiving portion (801), an LED displaying portion (803), a key matrix inputting portion (803) for adjustment, and a main board (453) from which an output is subjected to serial-to-parallel conversion.

The main board 453 of *Ichikawa* includes a function of converting the processed signals from serial to parallel form. Col. 21, lines 49-52. By contrast, the signal conversion section recited in claims 4, 8, and 10 processes the input signals in parallel column by column and outputs the processed signals in parallel. It is therefore not necessary in the apparatus of claims 4, 8, and 10 to convert the processed signals from serial to parallel form. Furthermore, the main board 453 of *Ichikawa* includes a single CPU for processing input signals. Col. 21, line 32. *Ichikawa* thus requires the CPU to process the input signals

at a higher rate. By contrast, the conversion section of claims 4, 8, and 10 processes the input signals in parallel column by column, so that the processing rate may be reduced.

The Examiner further asserts that *Ichikawa* teaches a signal transfer switch 327, which can be opened and closed according to the pulse from the shift register 321. The display section recited in claims 1 and 4, however, does not require circuitry corresponding to the shift register 321 because it is adapted to receive signals column by column.

Although the Examiner concludes that it would have been obvious for one having ordinary skill in the art to somehow modify *Itoh*'s imaging-displaying system in view of *Ichikawa*'s matrix inputting adjustment method, such an asserted modification (assuming the applied references may be combined, which Applicant does not admit) fails to satisfy the claim features discussed above.

At least in view of the above, Applicant respectfully requests reconsideration and withdrawal of the Examiner's rejection based on the applied combination of *Itoh* and *Ichikawa*.

CONCLUSION

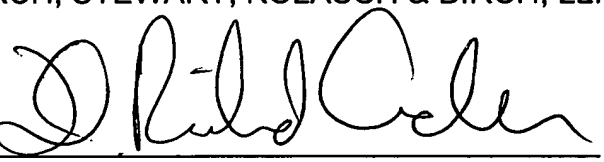
Should there be any outstanding matters which need to be resolved in the present application, we respectfully request the Examiner to contact the undersigned at (703) 205-8000, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for

any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By 
D. Richard Anderson, #40,439

P.O. Box 747
Falls Church, VA 22040-0747
(703) 205-8000

DRA/jdm
0378-0366P

Attachment: Version With Markings to Show Changes Made

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

The claims have been amended as follows:

1. (Three Times Amended) An image display apparatus comprising:

an imaging section which converts an optical image to [signal charges] signals, said imaging section including:

photoelectronic conversion devices arranged in the form of a matrix,

vertical transfer paths arranged adjacent to the respective columns of said photoelectronic conversion devices, each of said vertical transfer paths transfers signal charges toward a lower end in accordance with vertical driving pulses supplied from the outside,

transfer gates for transferring signal charges generated by said photoelectronic conversion devices to the respective vertical transfer paths in accordance with field shift pulses supplied from the outside respectively, and

output circuits for converting signal charges arrived at the lower ends of said vertical transfer paths to signals and outputting the signals in parallel column by column of said matrix; and

a display section which displays an image,

said display section including:

display devices arranged in the form of a matrix, each of said display devices has a signal input terminal and a control signal input terminal, and displays an image

represented by signals applied to the signal input terminal thereto at the time of application of driving pulses to the control signal input terminal,

input circuits for receiving signals output from said imaging section in parallel column by column and outputting signals corresponding the received signals to the signal input terminals of said display devices via signal buses in parallel column by column of said matrix, and

a vertical driving circuit for outputting the driving pulses to the control signal input terminals of said display devices via control buses line by line of said matrix in a predetermined order.

4. (Three Times Amended) An image display apparatus comprising:

an imaging section which converts an optical image to [signal charges] signals,

said imaging section including:

photoelectronic conversion devices arranged in the form of a matrix,

vertical transfer paths arranged adjacent to the respective columns of said photoelectronic conversion devices, each of said vertical transfer paths transfers signal charges toward a lower end in accordance with vertical driving pulses supplied from the outside,

transfer gates for transferring signal charges generated by said photoelectronic conversion devices to the respective vertical transfer paths in accordance with field shift pulses supplied from the outside respectively, and

output circuits for converting signal charges arrived at the lower ends of said vertical transfer paths to signals and outputting the signals in parallel column by column of said matrix;

a signal conversion section for performing a processing for the signals output from said imaging section in parallel column by column and outputting the processed signals in parallel; and

a display section which displays an image,

said display section including:

display devices arranged in the form of a matrix, each of said display devices has a signal input terminal and a control signal input terminal, and displays an image represented by signals applied to the signal input terminal thereto at the time of application of driving pulses to the control signal input terminal,

input circuits for receiving signals output from said signal conversion section in parallel and outputting signals corresponding the received signals to the signal input terminals of said display devices via signal buses in parallel column by column of said matrix, and

a vertical driving circuit for outputting the driving pulses to the control signal input terminals of said display devices via control buses line by line of said matrix in a predetermined order.

8. (Three Times Amended) An image display apparatus comprising:

an imaging section which converts an optical image to [signal charges] <u>signals</u>,

said imaging section including:

photoelectronic conversion devices arranged in the form of a matrix,

vertical transfer paths arranged adjacent to the respective columns of said photoelectronic conversion devices, each of said vertical transfer paths transfers signal charges toward a lower end in accordance with vertical driving pulses supplied from the outside,

transfer gates for transferring signal charges generated by said photoelectronic conversion devices to the respective vertical transfer paths in accordance with field shift pulses supplied from the outside respectively, and

output circuits for converting signal charges arrived at the lower ends of said vertical transfer paths to signals and outputting the signals in parallel column by column of said matrix;

a signal conversion section for performing a processing for the signals output in parallel from said imaging section column by column and outputting the processed signals in parallel; and

a parallel-to-serial conversion section for converting the signals output in parallel from said signal conversion section to serial signals.